What is Claimed is:

1. In a digital and analog broadcasting receiver comprising both a digital tuner for receiving digital broadcasting and an analog tuner for receiving analog broadcasting, a digital and analog broadcasting receiver comprising:

a first CPU; and

a second CPU,

the first CPU being in charge of existent station channel search processing on the side of the digital tuner,

the second CPU being in charge of existent station channel search processing on the side of the analog tuner,

channel searches by the first CPU and the second CPU being concurrently conducted.

2. The digital and analog broadcasting receiver according to claim 1, wherein

when the existent station channel search is started,

the first CPU instructs the second CPU to start the existent station channel search and performs the existent station channel search processing on the side of the digital tuner, and

the second CPU performs the existent station channel search processing on the side of the analog tuner

upon receipt of the instruction to start the search from the first CPU.

3. The digital and analog broadcasting receiver according to claim 1, wherein

the second CPU inputs a signal based on a key operation by a user and operates.

4. The digital and analog broadcasting receiver according to claim 2, wherein

the second CPU inputs a signal based on a key operation by a user and operates.

5. The digital and analog broadcasting receiver according to claim 1, comprising

a first memory; and

a second memory,

the first CPU controls the writing and read-out of channel information to and from a first memory, and

the second CPU controls the writing and read-out of channel information to and from a second memory.

6. The digital and analog broadcasting receiver according to claim 2, comprising

a first memory; and

a second memory,

the first CPU controls the writing and read-out of channel information to and from a first memory, and

the second CPU controls the writing and read-out of

channel information to and from a second memory.

7. The digital and analog broadcasting receiver according to claim 3, comprising

a first memory; and

a second memory,

the first CPU controls the writing and read-out of channel information to and from a first memory, and

the second CPU controls the writing and read-out of channel information to and from a second memory.

8. The digital and analog broadcasting receiver according to claim 4, comprising

a first memory; and

a second memory,

the first CPU controls the writing and read-out of channel information to and from a first memory, and

the second CPU controls the writing and read-out of channel information to and from a second memory.

9. The digital and analog broadcasting receiver according to claim 1, wherein

the second CPU feeds the channel information obtained in the existent station channel search processing to the first CPU, and

the first CPU manages all the channel information on one memory.

10. The digital and analog broadcasting receiver

according to claim 2, wherein

the second CPU feeds the channel information obtained in the existent station channel search processing to the first CPU, and

the first CPU manages all the channel information on one memory.

11. The digital and analog broadcasting receiver according to claim 3, wherein

the second CPU feeds the channel information obtained in the existent station channel search processing to the first CPU, and

the first CPU manages all the channel information on one memory.

12. The digital and analog broadcasting receiver according to claim 4, wherein

the second CPU feeds the channel information obtained in the existent station channel search processing to the first CPU, and

the first CPU manages all the channel information on one memory.